Claim 19 is directed to a programmable device adapted to be connected in parallel to two or more memory devices such that the programmable device is adapted to receive configuration data stored in the two or more memory devices without transmitting the configuration data via a controller connected between any of the memory devices and the programmable device, wherein the programmable device is adapted to receive a different portion of the configuration data from each different memory device.

In rejecting claim 19, the Examiner stated that "Smith teaches all claimed features in Fig. 2." In particular, according to the Examiner, Smith's FPGA **17** is an example of the programmable device of claim 19, and Smith's SDRAM banks 0 and 1 are examples of the two or more memory devices of claim 19. While it is true that Smith teaches FPGA **17** connected in parallel to SDRAM banks 0 and 1, where data can be transmitted from SDRAM banks 0 and 1 to FPGA **17** without transmitting that data via a controller connected between either of SDRAM banks 0 or 1 and FPGA **17**, Smith does not teach or even suggest all of the recitations of claim 19. In particular, Smith does not teach or suggest that the data stored in SDRAM banks 0 and 1 and transmitted to FPGA **17** is <u>configuration</u> data.

Configuration data is a special type of data that is used to initially program a programmable device, such as an FPGA. Prior to configuration, an FPGA is an unprogrammed device whose only (relatively limited) functionality is encoded in hardware (i.e., not software) on the FPGA. This limited non-software-based functionality includes the ability to receive configuration data in a particular format at a particular set of one or more input pins in order to program the FPGA to enable the FPGA to perform additional, <u>software-based</u> functions. Programmable devices, such as FPGAs, are therefore specifically designed to receive configuration data in particular formats at particular pins connected to circuitry that is specifically designed to support the initial programming of the device based on that received configuration data.

<u>None</u> of the data described in Smith being transmitted from SDRAM banks 0 and 1 to FPGA **17** is configuration data that would get transmitted to FPGA **17** <u>before</u> FPGA **17** was programmed. Rather, <u>all</u> of the data described in Smith as being transferred from SDRAM banks 0 and 1 to FPGA **17** is data that is transferred <u>after</u> FPGA **17** has been programmed. See, e.g., paragraph [0058] ("Software processes which require data from the memory of another processor node may 'post' or write a request into the memory of the other processor, where a task may be waiting in the other processor to explicitly move the data for the requesting task."); paragraph [0068] ("the programmed FPGAs **(17)** provide DMA engines that can automatically move data to and from the processors **(11)**"); paragraph [0069] ("software processes may access the local and remote memories"); paragraph [0076] ("the programmed FPGAs provide DMA engines for moving data in and out of the various local memories via the six communications paths **(100, 18, 19, 103, 104)** and the board I/O busses").

There is no teaching or even suggestion anywhere in Smith that SDRAM banks 0 and 1 store configuration data, where FPGA **17** receives a different portion of the configuration data from each different memory device. As such, Smith does not anticipate claim 19, which explicitly recites that "the programmable device is adapted to receive a different portion of the configuration data from each different memory device."

For all these reasons, the Applicant submits that claim 19 is allowable over Smith. For similar reasons, the Applicant submits that claims 34-35 are also allowable over Smith. Note further that claim 35 explicitly recites "configuring the programmable device using the configuration data," which Smith does not teach. The Applicant submits therefore that the rejections of claims under Sections 102(e) have been overcome.

In view of the above remarks, the Applicant believes that the pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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